Differential & Multistage Amplifiers

A journey of a thousand miles
begins with
a single step.

Lao – tzu *Chinese philosopher*
(604 BC - 531 BC)

Differential & Multistage Amplifiers

- Move to more complex analogue circuits and systems.
- Differential Amplifiers
  - Most widely used building block
  - Input stage of every op-amp
- These are well-suited for IC fabrication because:
  - Performance depends on matching the two sides of the pair
  - These utilize more components than single-ended circuits and are economical in IC fabrication
- Why differential amplifiers?
    - Less sensitive to noise and interference
      - If there is interference on the two input wires, the difference only is sensed (interference cancels out)
    - Direct coupling is possible thus large capacitances can be avoided
    - So ideally suited for IC fabrication because large capacitors are difficult to fabricate economically in IC process
- …contd!

Difference / Differential Amplifiers

- **What is a difference amplifier?**
  - **A difference amplifier is one that responds to the difference between the two signals applied at its inputs.**
    - **It ideally rejects signals that are common to both inputs.**
- **Consider the input signals as v_1 and v_2 :**
  - **The difference / differential input signal is:**

$$v_{Id} = v_2 - v_1$$

  - **The common-mode input signal is the average of the two input signals:**

$$v_{Icm} = (v_2 + v_1)/2$$

- **By adding and subtracting to get v_1 and v_2 :**
  - $v_1 = v_{Icm} - (v_{Id})/2$ **and**
  - $v_2 = v_{Icm} + (v_{Id})/2$

- **Pictorially!**
- **Example : Determine the differential and common-mode input signals when the two inputs are v_1 = 1.002 V and v_2 = 0.998 V.**
- **Solution: v_{Icm} = 1 V and v_{Id} = - 4 mV**

- **Output of a Difference/Differential Amplifier!**

Output of a Difference Amplifier

- Ideally the difference amplifier will amplify only the differential input signal $v_{Id.}$
- It will completely reject common-mode input signal $v_{Icm.}$
- However, non ideal or practical circuits will have an output voltage :

$$v_o = A_d v_{Id} + A_{cm} v_{Icm}$$

where A_d denotes amplifier differential gain and A_{cm} denotes common-mode gain

- A parameter that determines efficacy of a differential amplifier is defined as Common-Mode Rejection Ratio:

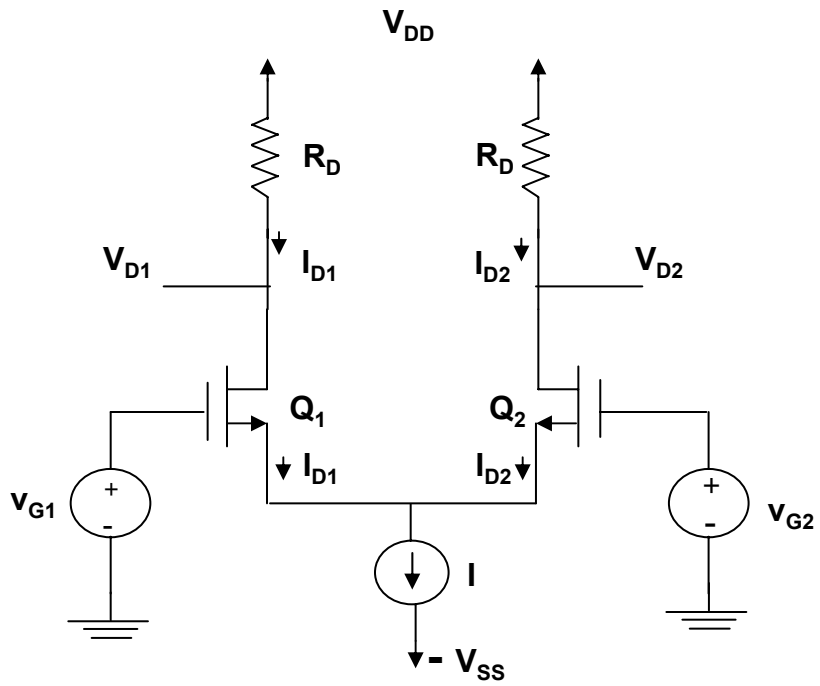
$$CMRR = 20 \log \{A_d / A_{cm}\}$$

  - Ideally CMRR is infinite because $A_{cm} = 0$
- Where does the common-mode signal come from?

- The MOS Differential Pair!

The MOS Differential Pair

- The circuit for basic MOS differential pair is :
- Two matched MOS transistors Q_1 and Q_2 with sources joined together by a constant current source I.
- Operation is such that MOSFET does not enter in triode region of operation.
- Generally active loads are employed instead of R_D.
- Various modes of operation are possible:
  - Operation with a common-mode input voltage
  - Operation with a differential input voltage
  - Large signal operation
  - Small-signal operation



- Operation with a common-mode input voltage!

Operation with a Common – Mode Input Voltage

- The circuit:
- The two gates are joined together and connected to a voltage v_{cm} called the common-mode voltage
- So $V_{G1} = V_{G2} = V_{CM}$
- And $V_S = V_{CM} - V_{GS}$
- Since Q_1 & Q_2 are matched $i_{D1} = i_{D2} = I/2$
- V_{GS} is gate to source voltage corresponding to a drain current of I/2
- Neglecting channel length modulation, the drain current is:

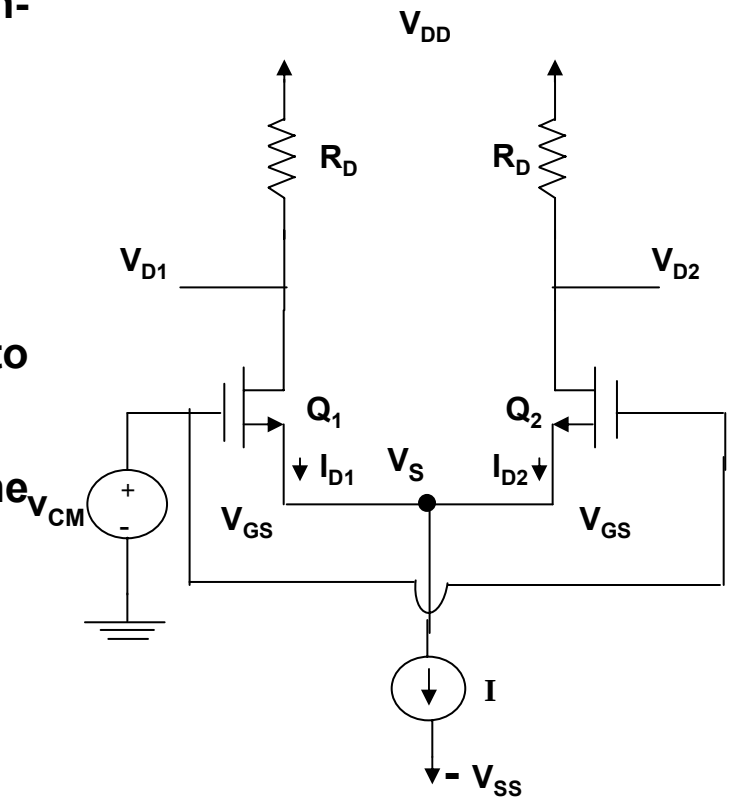
$$I_{D1} = I_{D2} = \frac{I}{2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) \left(V_{GS} - V_t\right)^2$$

- Or:

$$\frac{I}{2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) \left(V_{GS} - V_t\right)^2 = \frac{1}{2} k_n' \left(\frac{W}{L}\right) \left(V_{ov}\right)^2$$

- And:

$$V_{ov} = \sqrt{\frac{I}{k_n' \left(\frac{W}{L}\right)}}$$



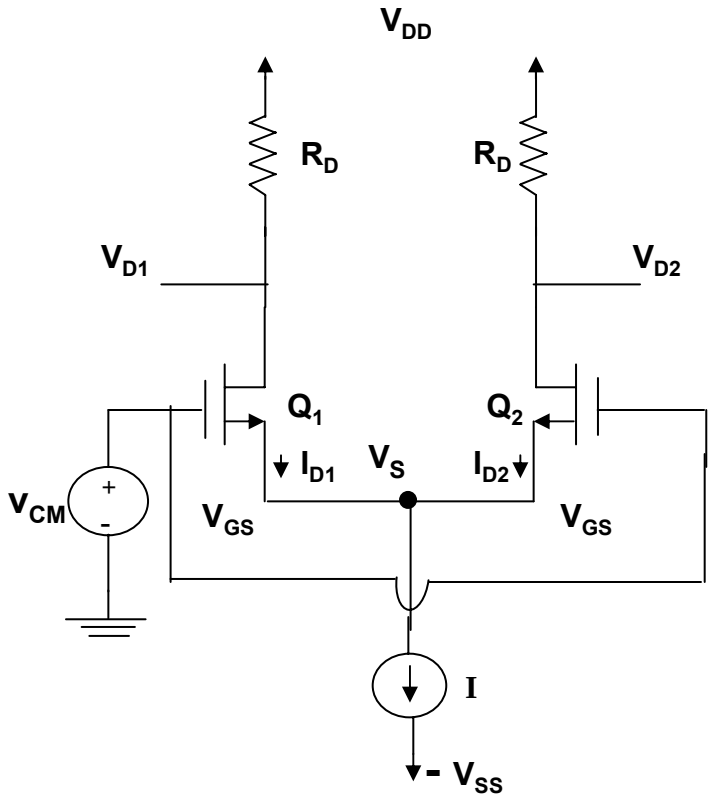
- Operation with a common-mode input voltage…contd!

Operation with a Common – Mode Input Voltage…contd

- The voltage at each drain:

$$V_{D1} = V_{D2} = V_{DD} - I/2R_D$$

- The difference in voltage of two drains is zero.
- The differential pair does not respond to (it rejects) common-mode i/p signals.
- Varying the value of v_{cm}, current I continues to divide equally between Q_1 and Q_2 as long as the transistors remain in saturation.
- The voltages at the drain will not change.



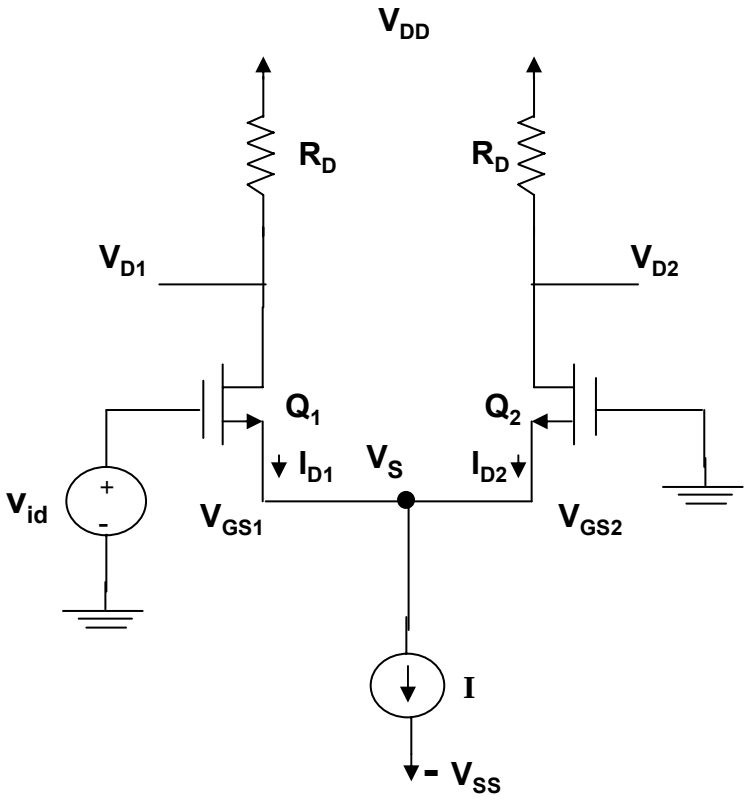
- Operation with a differential input voltage!

Operation with a Differential Input Voltage

- The circuit:
- We apply a difference or differential input voltage: $V_{id} = V_{GS1} - V_{GS2}$
- If V_{id} is positive, V_{GS1} will be greater than V_{GS2} and hence $i_{D1} > i_{D2}$
- The difference output voltage $V_{D2} - V_{D1}$ will be positive and vice versa when V_{id} is negative.
- So the differential pair responds to difference-mode or differential input signals.
- At some value of v_{id}, the entire bias current will flow in one of the two transistors.
  - For example; when v_{GS1} reaches the value that corresponds to:

$$i_{D1} = I = \frac{1}{2} k_n' \left(\frac{W}{L}\right) \left(V_{GS1} - V_t\right)^2$$

- …contd!



Operation with a Differential Input Voltage…contd

$$i_{D1} = I = \frac{1}{2} k_n' \left(\frac{W}{L}\right) \left(V_{GS1} - V_t\right)^2$$

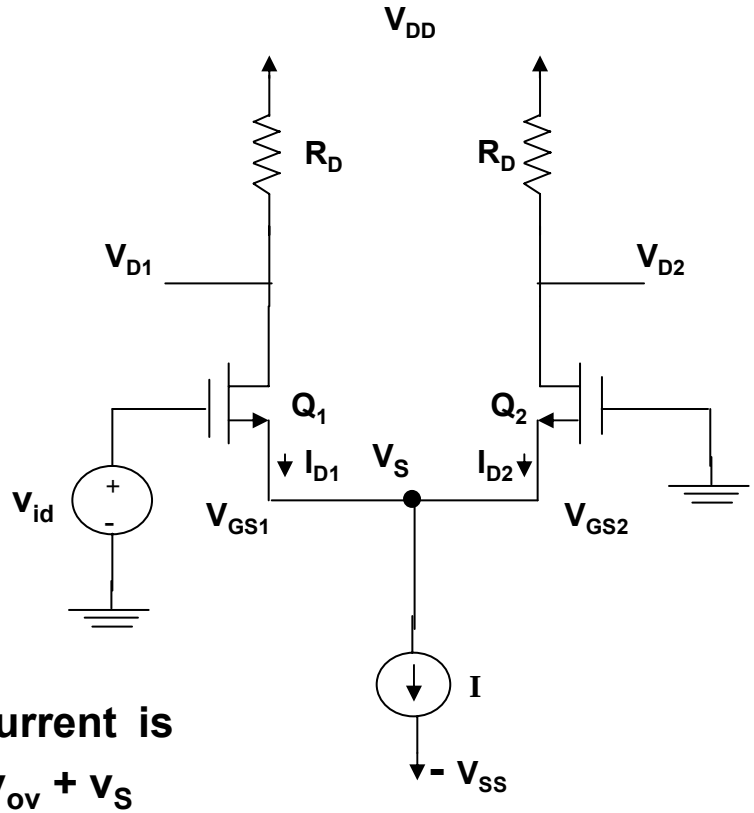
- **So:**

$$V_{GS1} = V_t + \sqrt{\frac{2I}{k_n' \left(\frac{W}{L}\right)}}$$

- **Or:**

$$V_{GS1} = V_t + \sqrt{2}\, V_{ov}$$

where v_{ov} is the overdrive voltage corresponding to a drain current of I/2.



- **The value of v_{id} at which the entire bias current is steered into Q_1 is $v_{idmax} = v_{GS1} + v_S = v_t + \sqrt{2}\, v_{ov} + v_S$**
- **Now $v_s = -v_t$ for cutting off Q_2.**
- **Hence $v_{idmax} = \sqrt{2}\, v_{ov}$**
- **And in the negative direction $v_{idmax} = -\sqrt{2}\, v_{ov}$**
- **Therefore the range is?**
- **Differential Amplifier as a linear amplifier!**

Operation as a Linear Amplifier

- Use of differential amplifier as a linear amplifier?
- Keep input signal small.
- This small signal increases current in one transistor and decreases proportional current in the other transistor by an amount ΔI.
- So current becomes $I/2 + \Delta I$ and $I/2 - \Delta I$
- A voltage signal $-\Delta I R_D$ and $+\Delta I R_D$ develops at the other transistor.
- The output voltage taken between the two drains will be $2 \Delta I R_D$ which is proportional to differential input signal v_{id}.

- Large –signal operation!